"Textured" Network Devices: Overcoming Fundamental Limitations of Nanotube/Nanowire Network-Based Devices**

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Single-walled carbon nanotubes (swCNTs) and nanowires are strong candidate materials for next-generation devices such as high-mobility field-effect transistors (FETs),[1–4] ultrasensitive sensors,[5–7] and so on.[8] One approach for practical device applications can be thin-film devices based on nanotube/nanowire networks.[9–22] However, such network-based devices have been suffering from various fundamental limitations. For example, transistors based on swCNT networks usually have a poor on–off ratio due to metallic swCNTs in the network channels.[10,16,18] Furthermore, nanotube/nanowire network-based devices in general exhibit low mobility and conductivity with nanoscale channel width due to the poor scaling behavior of percolated network channels.[13,19] Herein,

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we present a strategy to solve these fundamental problems simply by controlling the connectivity of swCNT/nanowire networks. In this strategy, "textured" network channels were prepared via the directed assembly method[20–23] and they were utilized to fabricate high-performance network-based devices. Using this strategy, we significantly improved the yield of swCNT network-based FETs with a large on–off ratio without removing metallic swCNTs. Polarized Raman spectroscopy was used to systematically investigate the structures of the textured network devices.[24] Significantly, both experimental and simulation results showed that the conductivity and mobility of textured network devices increased with reduced line width, unlike random network-based or conventional silicon-based devices. It indicates that our strategy can be an ideal solution for the fabrication of nanoscale devices based on swCNT/nanowire networks.

Figure 1 shows the schematic diagram depicting the procedure to prepare devices with random or textured swCNT network channels. The basic procedure is similar to that reported previously.[22] In brief, an octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM) with non-polar terminal groups was patterned on a SiO_2 surface using photolithography or e-beam lithography.[22–23] When the substrate was placed in the swCNT suspensions (usually $0.1 \, mg \, mL^{-1}$ in o-dichlorobenzene), swCNTs were selectively adsorbed onto bare SiO_2 regions up to a full monolayer due to the "self-limiting" mechanism.[22,25] We used swCNTs grown via the HiPCO method whose average length was ≈650 nm. Significantly, swCNTs adsorbed on the substrate self-align to stay only inside the bare surface regions without any external forces. In this case, the final structures of assembled swCNT networks were determined by the shape of surface molecular patterns. When the channel width was much larger than the length of individual swCNTs, swCNTs assembled mostly in random orientation forming random network channels. The textured network channels were prepared using multiple parallel line-shape patterns with an individual line width much smaller than the swCNT length. Note that in the previous method, thin films comprising randomly oriented swCNTs were etched to prepare device channels with the desired line width, which always resulted in randomly oriented swCNT networks. After the assembly of swCNT networks, we performed additional photolithography to fabricate electrodes

Figure 1. Schematic diagram depicting the fabrication procedure of FETs based on random or textured swCNT network channels.

topography imaging by dividing the swCNT volume by the pattern area.[22,26] The devices were categorized into three groups: 1) disconnected, 2) semiconducting, and 3) metallic. "Disconnected" devices represent the devices with maximum source–drain currents smaller than 10^{-10} A. If a device had an on-current larger than 10^{-8} A and turned off completely with an off-current smaller than 10^{-10} A, as in Figure 2a, the devices were categorized as "semiconducting" devices. "Metallic" devices are swCNT junctions with an off-current larger than 10^{-10} A as in Figure 2b. For transistor applications, the semiconducting devices are desirable.

The theoretical modeling was performed via Monte Carlo simulations, in which sticks representing swCNTs were randomly generated in the channel area with the same length distribution as that used in experiments (their average length is about 650 nm). Similar to our experiments, where swCNTs self-aligned to stay within the channel area, the orientations of simulated swCNT sticks near edges of the channel area were adjusted. We assumed that one third of swCNTs have metallic properties. Then, the current paths between source and drain were identified. It should be noted that a current path consisting only of metallic swCNTs should have metallic properties, while a path including at least one semiconducting swCNT should exhibit semiconducting properties. Thus, if at least one metallic path was identified in the device channel, the device was considered metallic because it did not turn off completely. On the other hand, devices with only semiconducting paths were identified as semiconducting ones. To match theoretical simulation results with experiments, in which the thickness of the swCNT network was measured via AFM, the effective thickness of the theoretical data was estimated by assuming that the diameter of a swCNT was ≈ 1.5 nm and calculating the volume of all swCNTs in the channel (Figure S1 of the Supporting information).[22,26] Note that our simulations were performed under a few assumptions: i) no broken swCNTs were generated; ii) junctions between swCNTs were modeled as simple ohmic contacts; and iii) bundling of swCNTs was not considered. These assumptions may be sources of small discrepancy from our experimental results, as shown in Figure 2c and d and described below.

The result in Figure 2c can be understood from standard percolation behaviors of swCNT networks. At a small thickness ($t_{\mathrm{eff}} < \approx 0.2$ nm), there were not enough swCNTs to form a complete current path between source and drain electrodes, and most junctions were "disconnected" (black blocks and lines in Figure 2c). As the swCNT density increased (0.2 nm $< t_{\mathrm{eff}} < 0.5$ nm), the complete current paths began to form between the electrodes. In this case, since swCNT networks usually contained more semiconducting swCNTs than metallic ones, semiconducting paths formed first, and the devices had good FET characteristics (blue blocks and lines in Figure 2c). In this intermediate thickness range, we could achieve high-performance transistors that could be turned off completely. At a large thickness, metallic paths were formed, and the devices exhibited metallic behavior (red blocks and lines in Figure 2c). This result indicates that one can achieve high-performance FET devices using a mixture of metallic and semiconducting swCNTs simply by controlling the thickness of

of 20-nm-thick Pd. The back-gate bias voltage was applied through a 100-nm-thick SiO_2 layer to measure transistor behaviors.

Figure 2a and b shows two typical gating effects of swCNT network-based FETs. Under ambient conditions, semiconducting swCNTs exhibit p-type semiconducting properties. Thus, a swCNT network channel with only semiconducting current paths should exhibit p-type semiconducting behavior with very low off-currents ($< 10^{-10}$ A) as in Figure 2a. However, swCNT network channels may contain both semiconducting and metallic current paths due to some metallic swCNTs. Since metallic paths do not respond to the gate bias voltage, the FETs based on such channels should exhibit metallic behavior with rather large off-current ($\gg 10^{-10}$ A), as seen in Figure 2b.

Figure 2c shows the distribution for electrical characteristics of swCNT network channels depending on swCNT film thickness. The blocks and lines in the graph represent experimental and theoretical simulation results, respectively. More than one hundred FETs with 16-μm-wide and 20-μm-long swCNT network channels were investigated to obtain the distribution. The effective thickness t_{eff} of the swCNT network channels was estimated from atomic force microscopy (AFM)

Figure 2. a) A typical gating effect of swCNT network channels with semiconducting behavior. Note that the channel has an off-current smaller than 10^{-10} A. b) A typical gating effect of swCNT network channels with metallic behavior. Note the channel did not turn off even with a large gate bias. c) Distribution of the electric characteristics of 16-μm-wide and 20-μm-long channels depending on the effective thickness of swCNT network layer. Black, blue, and red blocks represent the probability of having devices with disconnected, semiconducting, and metallic behaviors, respectively. In total, 112 CNT-FETs were tested. The lines represent theoretical simulation results. d) Distribution of the electric characteristics of 3-μm-wide and 20-μm-long channels depending on the effective thickness of swCNT network layer. Black, blue, and red blocks represent the probability of having devices with disconnected, semiconducting, and metallic behavior, respectively. In total, 120 CNT-FET devices were tested. The lines represent theoretical simulation results. e) Micro-Raman spectroscopy results taken at the boundary of 16-μm-wide CNT network channel. Blue and red lines represent the Raman spectra using both the incident and the scattered laser light with parallel and normal polarization, respectively. Black line represents the normalized Raman intensity I_p/I_{n-G}, where I_p and I_{n-G} represent the Raman intensity with parallel polarization and the G-band Raman intensity with normal polarization, respectively. f) Normalized Raman intensity I_{p-G}/I_{n-G} of micro-Raman data taken at various locations across the 16-μm-wide CNT network channel.

density of swCNT networks limits the current level of fabricated devices.

swCNT FETs with narrower channel width of $\approx$3 μm exhibited qualitatively similar behavior as those with 16-μm-wide channels (Figure 2d). However, the desirable thickness range with more semiconducting FETs than metallic ones increased to $\approx$0.2–0.7 nm, which is $\approx$50% broader range than previous results ($\approx$0.2–0.5 nm) in Figure 2c. A plausible explanation can be enhanced serial connectivity due to the alignment of swCNTs in the narrow channel (Figure S2 in Supporting Information).[12,14] Let's assume a device with multiple separate current paths in the channel. If all the paths contain, at least, one semiconducting swCNT, they will have semiconducting behavior, and the device will be a "semiconducting" one. However, if there are lateral connections between current paths, a metallic path can exist even when each path has, at least, one semiconducting swCNT (Figure S2 in Supporting Information). Thus, the ideal channels for high-performance FETs should be the textured network channels that comprise separate current paths without any connection between individual paths (Figure 1). It also implies that even in rather wide random network channels, the alignment of swCNTs along the channel direction improves the serial connections between electrodes and reduces the lateral connections between current paths, which should significantly enhance the probability of semiconducting paths. In our fabrication process, swCNTs were assembled only in the bare surface regions. Thus, the swCNTs in a narrow channel tend to align along the channel direction,[25] which, in effect, should enhance the probability of semiconducting devices (Figure 2c and d).

For more systematic analysis, we utilized the polarized Raman spectroscopy technique to quantify the degree of alignment of swCNTs in the network channel (Figure 2e). According to the Raman selection rule, both the incident and the scattered laser light polarized parallel to swCNT length direction can result in CNT Raman signals while Raman scattering is forbidden when both the incident and the scattered laser light are polarized normal to the swCNT length direction. The blue or red lines in Figure 2e represent the G-band Raman spectra using the laser light with polarization parallel or normal to the direction of the swCNT network channel, respectively. Since the swCNTs near the pattern boundary tend to align along the channel direction to stay inside the bare surface regions, the

swCNT films, as reported before.[18] In this case, it is highly desirable to achieve the thickness with more semiconducting devices than metallic ones. However, in Figure 2c, the desirable thickness range with more semiconducting devices than metallic ones seems narrow ($\approx$0.2–0.5 nm), which is problematic in achieving high yield for the fabrication of swCNT-based integrated devices. Furthermore, such low

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Raman intensity I_p with parallel polarization configuration exhibited much larger intensity than the Raman intensity I_n with normal polarization configuration. In this case, the normalized Raman intensity I_p/I_{n-G} can be utilized to quantify the degree of swCNT alignment in the network films, where I_{n-G} represents the maximum value of I_n (black line in Figure 2e). For example, the maximum G-band Raman intensity I_{p-G}/I_{n-G} in the normalized Raman spectrum of I_p/I_{n-G} is expected to be ≈ 1.0 for randomly oriented swCNT networks because I_p should be nearly the same as I_n. As the swCNTs in networks align along the channel direction, I_n will decrease compared with I_p, and the I_{p-G}/I_{n-G} value will increase rapidly.

The details of swCNT alignment inside the channel can be investigated using micro-Raman experiments (Figure 2f). Here, we performed polarized micro-Raman experiments at twenty different spots across the 16-μm-wide channel, which allowed us to measure the degree of local alignment of the swCNTs inside the swCNT channel. Significantly, we observed rather large I_{p-G}/I_{n-G} up to ≈ 2.5 within 2–3-μm regions from the pattern boundary, while $I_{p-G}/I_{n-G} \approx 1.0$ in the middle of the channel. It implies that the swCNTs near the boundary of the network channel align well along the channel directions, while the swCNTs in the middle of the wide channel remained randomly oriented.[24] This result can explain why the devices

with 3-μm-wide channels had a higher probability of semiconducting devices than those with 16-μm-wide channels. In brief, as the channel width decreased, the portion of boundary regions with aligned swCNTs increased, and, as a result, the probability of semiconducting devices was enhanced.

We could further use this effect as a means to significantly improve the yield of high-performance FETs with a large on–off ratio. As a proof of concept, we prepared two types of swCNT-FET device with identical total channel width but different connectivity. The first type of FET contained a single 800-nm-wide channel (Figure 3a), while the second type had the textured network structures comprising four 200-nm-wide channels (Figure 3b). Both types of device had a 10-μm channel length. It should be noted that both types of device had an identical total channel width of 800 nm, while the second type with multiple 200-nm-wide channels had the textured networks with highly aligned swCNTs along the channel direction. In our assembly process, swCNTs were adsorbed onto the channel region up to the maximum saturated density of swCNTs due to the "self-limiting" mechanism.[25] All devices were prepared using network channels with saturated density of swCNTs (effective thickness ≈ 1.5 nm) adsorbed onto bare surface regions. It should be noted that devices with 16-μm-wide channels having such high swCNT density mostly exhibited metallic behavior (Figure 2c). Only 17% of our devices with a single 800-nm-wide channel exhibited semiconducting behavior with an off-current of less than 10^{-10} A (Figure 3c). Surprisingly, when we used four 200-nm-wide channels, $\approx 88\%$ of the fabricated devices exhibited good FET behavior, which is more than a five times improvment in device yield. The alignment of swCNTs in the channels was characterized via micro-Raman spectroscopy (Figure 3d). In the case of the 200-nm-wide channels, the Raman intensity I_n with normal polarization configuration substantially diminished, implying the high degree of alignment of swCNTs along the channel direction in the networks. This result indicated that the textured channel structures can be a powerful means to significantly improve the yield of high-performance FET devices while maintaining their current level.

Other important issues in swCNT network-based applications are the scaling behaviors of conductivity and mobility of the channels with reduced channel width. In previous fabrication methods of random-network transistors, a swCNT film was first prepared over the entire substrate area, and then swCNTs other than those on the channel regions were severed via various etching processes such as oxygen plasma or ion milling.[13,19] In this case, most swCNTs located on the boundary of

Figure 3. a) AFM topography of a single 800-nm-wide channel (random network channel). b) AFM topography of four 200-nm-wide channels (textured network channel). c) Distribution of electrical characterization of random and textured swCNT network channels. 83 out of 100 FET devices based on random network channel exhibited metallic behavior, while 74 out of 84 devices based on textured channels had semiconducting behavior. d) Typical polarized micro-Raman spectra of a single 800-nm-wide (top) and four 200-nm-wide (bottom) CNT network channels. The blue or red lines represent the data measured with both the incident and the scattered photons polarized parallel or normal to the channel direction, respectively.

Figure 4. Scaling behavior of textured CNT network devices. a) Experimentally measured (black squares) and c) simulated (black circular dots) on-current conductivity σ_{on} of swCNT network channels with various channel width w. All conductivity values were measured (or simulated) at −6 V gate bias. The log−log plots in the inserts show that the data can be fit well by the curve (red lines) with the scaling behavior of $\sigma_{on} \sim w^{-\upsilon}$, where $\upsilon = 0.2$ and 0.19 in (a) and (c), respectively. Dashed line represents the reference data reported before. b) Experimentally measured (black squares) and d) simulated (black circular dots) mobility μ of CNT network channels with various channel width w. The log−log plots in the inserts show that the data can be fit well by the curve (red line) with the scaling behavior of $\mu \sim w^{-\upsilon}$, where $\upsilon = 0.21$ and 0.23 in (b) and (d), respectively. Simulation data points were calculated by taking an ensemble average over more than 100 devices for a given width.

the channel were chopped, and the swCNT networks in the channel, in effect, significantly lose the connectivity resulting in poor conductivity at narrow channel width. It was reported that as the channel width w of randomly oriented swCNT networks was reduced, the conductivity σ of the channel significantly decreased as $\sigma \sim w^{1.53}$ (broken lines in Figure 4a).[19] Such behavior was explained by the conventional percolation theory. It can be a serious problem especially for the transistors with narrow line width. Significantly, we found that the conductivity σ of the swCNT networks fabricated by our method actually increased for reduced channel width w with the scaling behavior of $\sigma \sim w^{-0.2}$ (Figure 4a). This is completely opposite behavior to the conventional percolation theory. Presumably, in conventional percolation theory assumed randomly oriented network, while our textured devices align along the channels on its boundary.

Such behavior was also seen in our simulations ($\sigma \sim w^{-0.19}$, Figure 4c). The conductivity was calculated from the ensemble-averaged conductance over more than 100 simulated channels. The conductance of each channel was computed by constructing an equivalent circuit comprising different resistors and applying Kirchhoff's law. The model values used were as follows: the resistance R_m of metallic CNTs was given by $R_m/L = 4$ kΩ μm^{-1}, where L is the distance between two crossed junctions with other CNTs or such a junction and a contact with an electrode.[27] For

semiconducting CNTs, we used the conductance, $G_s = \mu_{NT} C_{NT} (V_{G0} - V_G)/L$,[27–29] where CNT capacitance per length C_{NT} is ≈60 aF, the single CNT mobility μ_{NT} ranges from ≈1000–2000 cm^2 V^{-1}s^{-1}, V_G is the gate voltage applied, and V_{G0} is the threshold gate voltage randomly chosen between −4 and +1 V for different semiconducting CNTs. A crossed junction between two CNTs and a contact at a metal electrode were modeled with resistance values of ≈40 kΩ and ≈50 kΩ, respectively.[30]

Our unique scaling behavior of the conductivity can be explained by the alignment of swCNTs along the channel directions in our devices.[12,14,16] In our method, swCNTs tend to align along the channel direction in a narrow channel device. Thus, source and drain electrodes are connected by the smaller number of swCNTs in narrower channel devices. In this case, narrower channel should have shorter effective current paths with fewer CNT–CNT junctions, which, in effect, resulted in enhanced conductivity of the channel.

We also investigated the scaling behavior of the mobility of the FET devices with various channel widths shown in Figure 4b (experiment) and Figure 4d (simulation). We used the classical mobility equation $\mu = (dI_{SD}/dV_G)(L^2/C_g)(1/V_{SD})$ and parallel plate model of the capacitance as in previous reports.[31] Here, L and C_g represent the channel length and gate capacitance, respectively. In simulation, we took an ensemble-averaged value of $\Delta I_{SD}/\Delta V_G$ over more than 100 channels. The result shows that the mobility of textured FET increased with decreasing channel width, which is actually opposite behavior to conventional Si-based FETs and other swCNT network transistors. Such behavior also can be attributed to the swCNT alignment in narrow channels. In narrow channels, source and drain were connected by smaller number of swCNTs, which effectively reduced the number of contacts between swCNTs and eventually enhanced the mobility. It is also interesting that the mobility showed a scaling behavior similar to the conductivity, which is actually expected considering our mobility equation. If we rewrite our mobility equation

$$\mu = \frac{dI_{SD}}{dV_G} \cdot \frac{L^2}{C_g V_{SD}} = \frac{d}{dV_G}\left(\frac{I_{SD}}{V_{SD}}\right) \cdot \frac{L^2}{C_g} = \frac{d}{dV_G}\left(\sigma \frac{tw}{L}\right) \cdot \frac{L^2}{C_0 \cdot (Lw)}$$
$$= \frac{d}{dV_G}(\sigma) \cdot \frac{t}{C_0}$$

where t and C_0 represent the channel thickness and gate capacitance per unit channel area, respectively. Since gate voltage V_G and C_0 do not change with reduced channel width w, mobility μ calculated using this equation should scale in a

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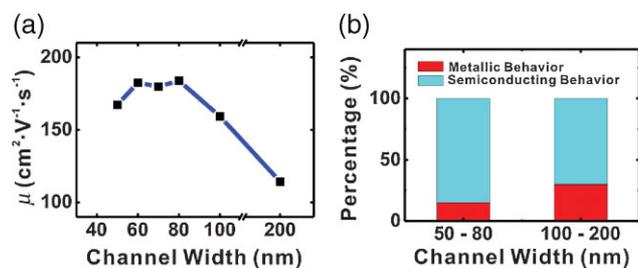
Figure 5. Submicrometer-wide network channel devices. a) Experimentally measured (black squares) mobility μ of CNT network channels with sub-200-nm channel width and 4-μm channel length. b) Distribution of electrical characterization of CNT devices with 50–80-nm width and 100-200-nm width. The channel length of the devices was 4 μm.

similar way as conductivity σ. Both experiments and simulations show, in both conductivity and mobility data, the onset of the deviation from the scaling behavior around $w \approx 8\,\mu$m, whose data points fall below the scaling curves. It appears that the absolute values of the exponents decrease and eventually approach a value observed in randomly oriented CNT networks[19] as the width increases, because CNTs are distributed more randomly in wider channels.

We also applied the same strategy to the submicroscale devices (Figure 5). The mobility of the devices with submicrometer channel width increased with reduced line width, and it saturated below ≈80-nm linewidth (Figure 5a). We also achieved a high yield of high-performance devices with a large on–off ratio (Figure 5b). These results show that our strategies can be utilized to achieve high-performance submicroscale devices.

In summary, we have presented a powerful strategy to overcome the fundamental limitations of network-based devices and to build high-performance nanoscale network devices. Here, surface molecular patterns were used to generate textured networks. The alignment of swCNTs in the networks effectively enhances the serial connectivity of swCNTs resulting in the significant enhancement of their overall on–off ratios. We could fabricate high-performance FETs with high yield ≈88% using textured network channels while maintaining high current level. Significantly, both experiments and simulations showed that the textured network channels enhance conductivity and mobility with reduced line width, which is a completely opposite behavior to randomly oriented swCNT networks or even conventional silicon-based devices. It indicates that this strategy can be an ultimate solution to solve the fundamental limitations for scaling down nanoelectronic devices.

Experimental Section

Surface molecular patterning: The photoresist (AZ1512) for micrometer-sized surface patterns and e-beam resist (ma-N 2401) for nanometer-sized surface patterns were first patterned on thermally SiO_2 (1000 Å) grown silicon substrates. As reported in References, [22,23] an octadecyltrichlorosilane (OTS) was utilized to pattern passivating molecular monolayer on SiO_2 surfaces. The

photoresist- or e-beam-resist-patterned substrates were dipped in the OTS solution (1:500 (v/v) in anhydrous hexane) for ≈100–200 s. To prevent OTS aggregation, the substrates were immediately rinsed with clean anhydrous hexane, and the photoresist or e-beam resist were removed with acetone.

swCNT network device fabrication: Purified swCNTs (Carbon Nanotechnologies) were sonicated in o-dichlorobenzene for 20 mins to prepare a swCNT solution. The OTS-patterned surface was placed in the swCNT solution. To obtain various effective thicknesses of swCNTs, different concentrations of swCNT solution and dipping periods of the substrate were utilized. After swCNT assembly, a typical lift-off process was employed to fabricate metal contact electrodes. The electrical characteristics of swCNT network devices were obtained by using a semiconductor characterization system (model: 4200-SCS, Keithley Instruments, Inc.)

Raman spectroscopy: Polarized Raman spectra were measured in the quasi-backscattering geometry with an Ar^+ laser (514.5 nm) as the excitation light source at room temperature. The scattered light was filtered with a holographic edge filter, dispersed by using a TRIAX 552 spectrometer, and detected with a liquid-nitrogen-cooled CCD detector. The spot size of the incident laser light for micro-Raman experiments was ≈1 μm.

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