Linker-free directed assembly of high-performance integrated devices based on nanotubes and nanowires

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Advanced electronic devices based on carbon nanotubes (NTs) and various types of nanowires (NWs) could have a role in next-generation semiconductor architectures. However, the lack of a general fabrication method has held back the development of these devices for practical applications. Here we report an assembly strategy for devices based on NTs and NWs. Inert surface molecular patterns were used to direct the adsorption and alignment of NTs and NWs on bare surfaces to form device structures without the use of linker molecules. Substrate bias further enhanced the amount of NT and NW adsorption. Significantly, as all the processing steps can be performed with conventional microfabrication facilities, our method is readily accessible to the present semiconductor industry. We use this method to demonstrate large-scale assembly of NT- and NW-based integrated devices and their applications. We also provide extensive analysis regarding the reliability of the method.

Recently, there has been a large amount of interest in new functional devices based on carbon nanotubes (NTs) and various types of nanowires (NWs)[1–13]. A lack of large-scale integration techniques has, however, been a major obstacle to the integration of those new devices into practical applications. Previous methods for device integration include the flow cell method[14], growth from catalyst patterns[15], dielectrophoresis[16,17] and others[18]. As some methods rely on external forces to align NTs or NWs, it is an extremely time-consuming task to integrate millions of NT- and NW-based devices with arbitrary orientations. Reactive linker molecules have also been used for the directed assembly of NTs and NWs[19–23], but it is known that the reactive chemical groups used for NT and NW adhesion could alter the electrical properties of the NTs and NWs in an unexpected manner[24].

In this paper, we report a molecular linker-free assembly method for assembling high-performance integrated devices based on NTs and NWs. In this method, inert surface molecular patterns guide the adsorption and alignment of NTs or NWs directly onto bare surface regions on the substrates, without relying on any external forces, and the substrate potential can be used to further enhance the NT and NW adsorption. As a proof of concept, we demonstrate large-scale assembly and alignment of single-walled carbon NTs (SWNTs) and V_2O_5 NWs on various solid substrates, including Au, SiO_2, glass, Si and Al, as well as fabrication of wafer-scale integrated devices such as a 64,000 array of SWNT junctions. Furthermore, we present high-performance transistors with an on–off ratio as large as $\sim 10^6$ achieved after selective breakdown of metallic SWNTs[25]. Importantly, as our method does not use a high-temperature process or any unconventional patterning equipment, it can be immediately applied by the present conventional semiconductor industry and may pave the way towards developing 'nanowire–silicon hybrid device' architectures.

ASSEMBLY OF NTs AND NWs ONTO A PRISTINE SUBSTRATE

Figure 1a is a schematic diagram depicting our assembly method. The first step comprises the patterning of a methyl-terminated self-assembled monolayer (SAM) onto solid substrates, leaving some parts of the bare surface regions unaltered. The methyl-terminated SAM patterns prevent the adhesion of NTs or NWs and direct their assembly of NTs and NWs towards the bare surface regions. We used 1-octadecanethiol (ODT) for Au substrates and octadecyltrichlorosilane (OTS) for surfaces with natural or grown oxide layers (for example, SiO_2, Si and Al) under ambient conditions. Molecular patterning was carried out using dip-pen nanolithography (DPN) for initial process development[26,27], and microcontact printing (μCP)[28] and photolithography methods[29] for large-scale patterning of ODT and OTS, respectively.

The patterned substrate was then placed in a solution of NTs or NWs for device assembly. The adsorption of NTs and NWs onto the patterned substrate depends on various factors, such as charges on the NTs and NWs and van der Waals interactions. SWNTs and V_2O_5 NWs are presented here as two typical examples (although we have recently found that the same strategy can be applied to other NWs such as ZnO and Si). SWNTs dispersed in 1,2-dichlorobenzene exhibit strong affinity to polar SAM patterns, but show minimal adhesion onto nonpolar SAM[19,20]. We found that SWNTs also show strong affinity to most bare surfaces (for example, Au, SiO_2, glass, Si and Al), presumably due to the natural polarization of pristine surfaces.

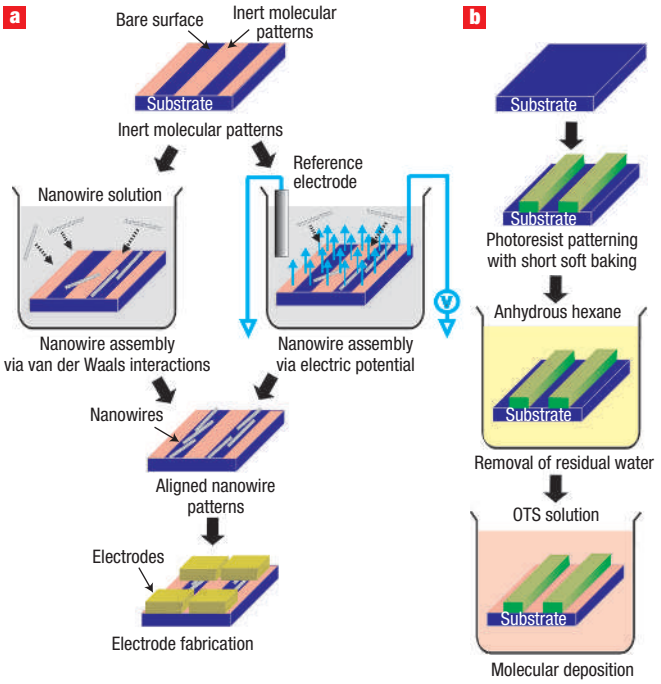

Figure 1 Schematic diagram of the NW assembly and molecular patterning method. a, The molecular linker-free assembly method. The inert molecular patterns drive the adsorption and alignment of NWs onto the bare surface regions on the substrate (left path); electric potential can be used to enhance NW adsorption (right path). **b**, The patterning process of OTS SAM on solid substrates (SiO_2, glass, Si, Al and so on) via photolithography. Unlike the conventional photolithography process, the baking time should be very short (<10 min at 95 °C), so the photoresist can be completely removed without any residue on the surface after molecular deposition.

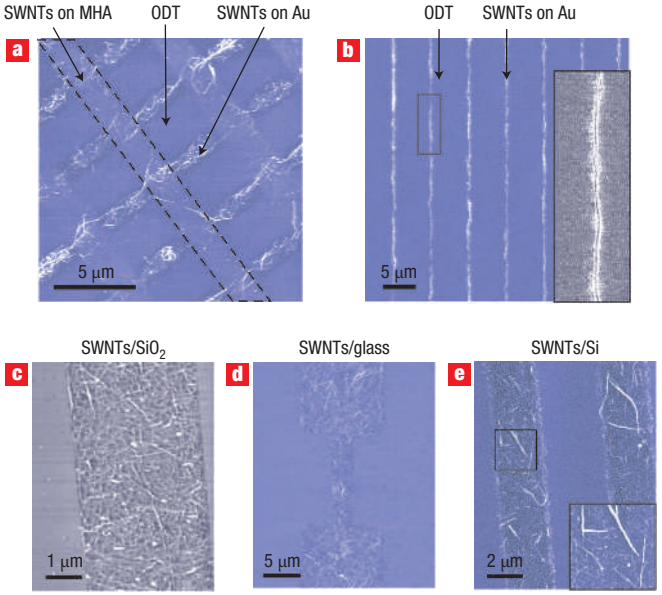

Figure 2 AFM topography images of SWNTs assembled directly onto bare substrates without any electric potential. a, SWNTs assembled onto surface molecular patterns comprising bare Au surface, MHA and ODT SAM regions. **b**, High-precision alignment of series of individual SWNTs onto bare Au surfaces using ODT as the nonpolar layer. The inset shows the lateral force microscope images of an individual SWNT (dark line), bare Au regions (bright area) and ODT regions (outside dark regions). **c**–**e**, SWNT networks formed directly on bare SiO_2 (**c**), glass (**d**) and Si (**e**) surfaces. OTS was used as the nonpolar layer.

This affinity can be used as a means to direct SWNT assembly. On the other hand, V_2O_5 NWs, which are negatively charged in aqueous solution, show minimal adsorption onto pristine surfaces. For this case, the electric potential was used to enhance NW adsorption onto the bare substrates. Here, we emphasize that the electric potential was used only to control the amount of NW adsorption, and the final shape of the assembled structures was completely determined by the shape of the bare surface regions. As the assembled NTs and NWs form stable structures, additional processing steps could be performed to fabricate NT- and NW-based devices. For example, additional microfabrication processes allowed us to build integrated electronic devices such as SWNT-based transistors (Fig. 1a).

One key procedure that makes this method immediately accessible to the conventional device industry is the molecular patterning method based on standard industrial microfabrication processes such as photolithography (Fig. 1b). In this process, photoresist is first patterned onto solid substrates with a short baking time (<10 min at 95 °C). Heating up the photoresist layer for a long time often results in residual photoresist on the substrates after development, which inhibits the formation of high-quality OTS SAM patterns. After photoresist patterning, the substrate is thoroughly rinsed with anhydrous hexane to remove residual surface water on the substrates. Under ambient conditions, water molecules are adsorbed onto polar surfaces, resulting in poor-quality OTS layers, such as multiple layer formation. After rinsing, the substrate is immediately placed in the OTS solution for selective passivation. Finally, the photoresist is removed with acetone. This method results in high-quality OTS layers, leaving some surface regions unaltered. Direct molecular patterning methods such as DPN and μCP are advantageous compared with the photolithography method owing to the simplicity of their processing steps. However, by patterning SAM via photolithography, we can take advantage of conventional microfabrication facilities.

ASSEMBLY OF SWNTs ON VARIOUS SUBSTRATES

Figure 2a shows the selective adsorption and alignment of SWNTs on surface molecular patterns composed of 16-mercaptohexadecanoic acid (MHA), ODT and bare Au regions. Interestingly, we found SWNTs adsorbed more on bare Au surfaces than on MHA, even though the polarization of the MHA surface was much stronger than that on Au. This is presumably a consequence of the slightly negative charges on SWNTs generated during the purification process using acids, reducing the affinity of SWNTs for the negatively charged MHA surfaces. Using only nonpolar ODT SAM patterns, we could achieve highly precise alignment of individual SWNTs without relying on any external forces (Fig. 2b). The results verify that the adhesive forces between SWNTs and bare surfaces are sufficiently strong to induce selective assembly, and thus align SWNTs with high precision. During our processes, SWNTs or NWs were always located in the bare surface regions. Therefore, the precision of NT and NW alignment by line-shape patterns can be estimated from the length of the NTs and NWs and the width of the bare surface regions. For example, assuming that a rigid NT

or NW with length l assembles onto a line-shaped bare surface region with width w, the maximum misalignment angle $\Delta\theta$ of the NT or NW is $\Delta\theta \approx w/l$.

This simple strategy has been applied to versatile substrates such as SiO_2, glass and Si (Fig. 2c–e). As bare surfaces usually have natural oxide layers, OTS could be used as the nonpolar SAM. It should be noted that conventional photolithography was used to pattern OTS layers for all the experiments (Fig. 1b). The atomic force microscope (AFM) images of Fig. 2 show uniform OTS SAM layers without multiple layer formation, implying the high quality of our SAM layers (Fig. 2c–e). It is clear that high-quality OTS SAM is critical in achieving high-precision alignment of SWNTs and avoiding non-specific adsorption onto the nonpolar area. SWNT patterns show uniform density and a clean boundary between the polar and nonpolar regions. It should be noted that clean bare surfaces without residual photoresist are a key requirement for high-quality SWNT patterns (Fig. 1b).

ASSEMBLY OF NTs AND NWs WITH ELECTRIC POTENTIAL

Electric potential was used to enhance the adsorption of NTs and NWs onto conducting substrates or those with thin insulating layers (Fig. 3). Figure 3a shows V_2O_5 NWs and SWNTs adsorbed onto various substrates with a bias voltage. For example, V_2O_5 NWs did not adhere to bare Si or SiO_2 surfaces without a bias voltage. As V_2O_5 NWs were charged negatively in aqueous solution, we could assemble them by applying positive substrate bias. On the other hand, SWNTs exhibited only weak adsorption onto Al, and we could enhance SWNT adsorption onto Al surfaces by applying substrate bias.

Figure 3b shows the amount of V_2O_5 NWs and SWNTs adsorbed onto Si substrates under different bias voltages. For quantitative analysis, we took five 10 μm × 10 μm AFM topography images from each sample and measured the volume of adsorbed NTs and NWs per unit area, which is termed here 'effective thickness'. Negatively charged V_2O_5 NWs were attracted towards Si surfaces under positive bias voltage, but exhibited no adsorption under negative or zero bias. However, SWNTs adhered to various bare surfaces without any bias due to van der Waals interactions. The effect of applied bias voltage for the SWNTs seems relatively small compared with V_2O_5 NWs. We have also observed similar behaviours on other surfaces (see Supplementary Information, Fig. S1).

In our experiments, the electric potential was used only to enhance the NT or NW adsorption, and the final structures of the adsorbed NTs and NWs were still completely determined by surface molecular patterns. On the contrary, in the dielectrophoretic methods previously reported, the electric field was used to control the final structures of the adsorbed NWs[16,17]. One interesting control experiment is the assembly of fluorinated SWNTs (Fig. 3c). Fluorinated SWNTs also show larger adsorption with substrate electric potential, just like unmodified SWNTs. Surprisingly, fluorinated SWNTs were assembled onto nonpolar ODT regions, but unmodified SWNTs adhered to bare Au regions. This result implies that the applied bias drove NTs towards substrates, but the location and alignment of adsorbed SWNTs were mainly determined by the interface properties between the SWNTs and substrates, and the shape of molecular patterns. In this way, we therefore have a means to control independently the density of adsorbed NTs and NWs and the final geometry of assembled NTs and NWs.

As applied bias voltages were used only to control the amount of adsorbed SWNTs and NWs, we could achieve high-precision alignment of SWNTs and NWs even with applied bias voltage. Figure 3d shows SWNTs assembled onto nanoscale-width bare surface regions with a passivating ODT layer. Furthermore, using small patterns with applied bias, we could even assemble individual V_2O_5 NWs onto the substrates (Fig. 3e).

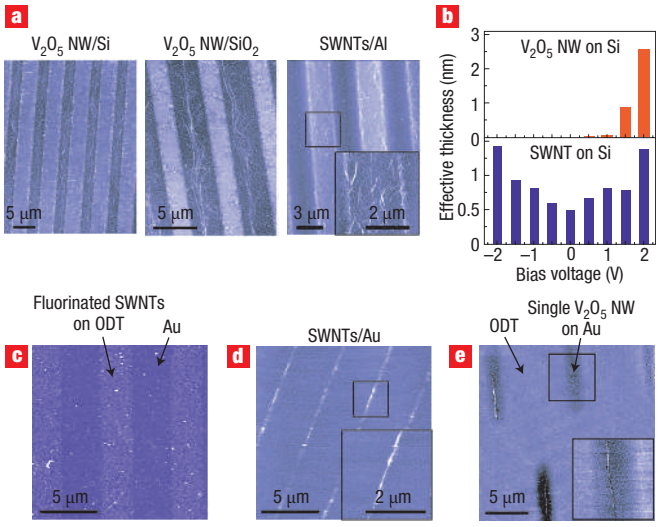

Figure 3 AFM topography images of SWNTs and V_2O_5 NWs assembled directly onto various bare surfaces with an electric potential. **a**, V_2O_5 NWs selectively adsorbed onto bare Si (left) and SiO_2 (middle) surfaces using a substrate bias of 3 V and 6 V, respectively. SWNTs selectively adsorbed onto bare Al surfaces with a substrate bias of −1.5 V (right). OTS was used for passivation. **b**, The effective thickness of adsorbed V_2O_5 NWs and SWNTs on Si under various bias voltages. **c**, Fluorinated SWNTs adsorbed onto ODT regions with −3 V substrate bias. **d**, High-precision alignment of SWNTs onto Au surfaces with −1 V substrate bias. ODT was used as the nonpolar layer. **e**, Selective adsorption of individual V_2O_5 NWs directly onto bare Au surfaces using 3 V substrate bias. ODT was used as the nonpolar layer.

LARGE-SCALE FABRICATION OF NT- AND NW-BASED DEVICES

Once NTs and NWs adsorb onto bare surfaces and form stable structures, we can introduce additional processing steps to fabricate more-complicated device structures. As a proof of concept, we fabricated millions of junctions connected by SWNT network patterns (left image of Fig. 4a) and 64,000 (256 × 256) junctions comprising individual or a few SWNTs (right image of Fig. 4a). Here, OTS patterns directed the assembly of SWNTs onto bare SiO_2 surfaces, and then electrodes were fabricated using photolithography and the lift-off method. Importantly, as all the steps, including OTS patterning, can be performed by conventional microfabrication processes, we could achieve wafer-scale fabrication of integrated devices based on SWNTs (left image of Fig. 4b). Furthermore, because our method does not involve any high-temperature processing steps, we could apply it to soft substrates such as glass (right image of Fig. 4b). The results clearly show that our method is readily usable by conventional microelectronics industry for large-scale fabrication of integrated devices based on SWNTs and NWs on virtually all general electronic substrates, possibly including those with preexisting circuit structures.

We were also able to coat the fabricated SWNT junctions with a thin SiO_2 layer using plasma-enhanced chemical vapour deposition and added gate electrodes on top of them to build

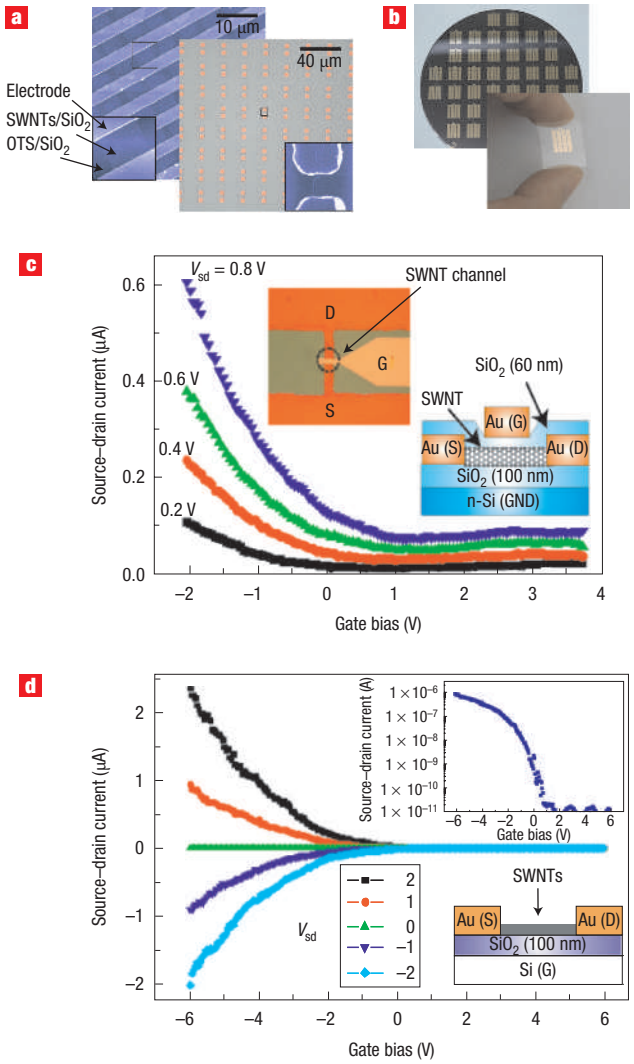

Figure 4 SWNT junctions and their gating effects. a, AFM topography images of multiple junctions connected by SWNT networks (left) and optical micrograph image of 64,000 (256 × 256) junctions with individual and a few SWNTs (right). The inset shows an AFM topography image of a single junction. **b**, Wafer-scale fabrication of SWNT junctions on a SiO_2 wafer (left) and cover glass (right). **c**, Gating effect of a top-gate transistor (with 3-μm-width; 4-μm-length SWNT network channel) under different source–drain voltages (V_{sd}). The insets show the optical micrograph image (left) and the cross-sectional structure of the transistor (right) where S is the source, D the drain, G the gate, and GND the ground. **d**, Gating effect of a high-performance SWNT transistor (with 3-μm-width; 4-μm-length network channel) after selective breakdown of metallic SWNTs. The Si substrate was used as a back-gate. Insets show the log-scale plot of the gating effect (top) and the cross-sectional structure of the transistor (bottom).

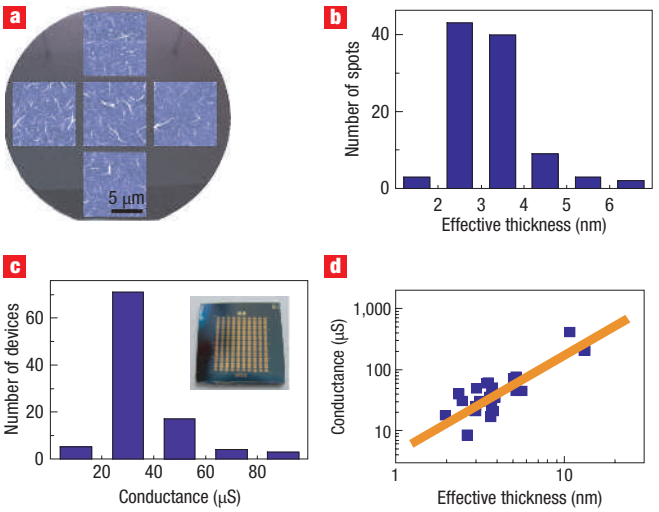

Figure 5 Uniformity of assembled devices. a, AFM topography images of SWNTs adsorbed onto five different locations (top, bottom, centre, right and left) of a 4-inch SiO_2 wafer. **b**, Distribution of the effective thickness of SWNT layers adsorbed onto the 4-inch SiO_2 wafer. The effective thickness was measured using AFM on 100 different locations distributed randomly over the wafer. **c**, Distribution of the conductance of 100 SWNT junctions with Au/Pd electrodes. In each junction, two electrodes with a 4-μm gap were connected by 3-μm-wide SWNT patterns. The inset shows the optical micrograph image of the junctions. **d**, Log–log plot of conductance versus effective thickness of SWNT junctions with Au/Pd electrodes on SiO_2 substrates. The slope of the log–log plot was found to be 1.49.

top-gate transistors that could be turned off individually. Figure 4c depicts the optical micrograph image of a top-gate transistor based on SWNT networks and its gating effects. Surprisingly, the yield of the top-gate transistors in our method exceeded 95%. The transistors exhibited typical *p*-type behaviour, with the source–drain current increasing at negative gate bias, but decreasing as gate bias increased positively. Furthermore, at a large positive gate bias, the source–drain current increased slightly, implying weak ambipolar behaviour, as often observed in top-gate transistors in previous works[30]. The current was not turned off completely, because metallic SWNTs were adsorbed together with the semiconducting SWNTs, which meant a current was always flowing through the metallic SWNTs. For high-density electronics applications, one still needs a high-yield method for the separation of metallic and semiconducting SWNTs. However, our method, at least, allows us to completely integrate SWNTs with present Si-based microelectronics and should immediately open up several industrial applications such as sensors. One application, the use of SWNT-based biosensors to detect glutamate, a neurotransmitting material, is provided as an example (see Supplementary Information, Fig. S3). In this case, SWNT junctions were functionalized with the enzyme glutamate oxidase. When the junctions were placed in the solution containing glutamate, glutamate was oxidized by the attached enzyme and changed the conductivity of the SWNT junctions, enabling real-time detection of glutamate. We could also fabricate V_2O_5 NW-based devices such as back-gate transistors (see Supplementary Information, Fig. S2) and demonstrate the n-type gating effect as reported before[29].

Although the lack of a high-yield method for separating semiconducting SWNTs from metallic ones prevented us from fabricating high-performance transistors at the wafer level, we successfully accomplished the fabrication of high-performance transistors at device level using the selective breakdown method[25]. We applied a 12 V source–drain voltage bias with 6.5 V gate bias, where the p-type semiconducting SWNTs are believed to be completely turned off, to burn selectively the metallic SWNTs after the fabrication of SWNT network junctions with Pd electrodes. Consequently, the current flowed mainly through the metallic SWNTs, and thus selectively burned the

metallic SWNTs. After applying source–drain voltage bias for a specific time (~10 min), we could obtain high-performance transistors with an on–off ratio as large as $\sim 10^6$, as shown in Fig. 4d. This result clearly shows that our method can be used for the fabrication of high-performance integrated circuits based on SWNTs.

UNIFORMITY OF ASSEMBLED DEVICE STRUCTURES

One extremely important criterion in applying a fabrication method for industrial applications is its reliability. We performed extensive analysis of the uniformity of fabricated structures and the yield of our method. Figure 5a shows typical AFM topography images of SWNTs adsorbed on a 4-inch SiO_2 wafer. The wafer was dipped in the 0.1 mg ml^{-1} SWNT solution for 5 s for SWNT adsorption. The images taken on the top, bottom, centre, right and left regions on the 4-inch wafer showed a similar density of SWNTs, implying the uniformity of assembled SWNT structures obtained when using our method.

For quantitative analysis about uniformity, AFM topography images (10 μm × 10 μm) were taken at 100 different locations distributed randomly over the 4-inch wafer, and the effective thickness was measured from each AFM image. The distribution of measured effective thickness of adsorbed SWNTs is shown in Fig. 5b. The results show that we achieved SWNT films with effective thickness of ~3.23 nm with a standard deviation of ~1.14 nm. It is clear that our method can produce a uniform SWNT layer over wafer scale. The standard deviation of the effective thickness should depend on factors such as the distribution of SWNT diameters, the stochastic variation of NT adsorption, and so on. One important parameter can be the dispersion of the SWNT solution. In the solution, SWNTs often form large bundles, which significantly reduce the uniformity of adsorbed SWNT structures. When we excluded AFM images with SWNT bundles larger than 10 nm, we could achieve an effective thickness ~3.15 nm with a standard deviation of ~0.827 nm. The results imply that the uniformity can be further improved by further controlling the dispersion of our SWNT solution.

We also assembled SWNTs onto specific locations on SiO_2 substrates using OTS patterns and added Au/Pd (Fig. 5c) or Au/Ti (see Supplementary Information, Fig. S4) electrodes to fabricate SWNT junctions. In each junction, two electrodes with a 4-μm gap were connected by 3-μm-wide SWNT patterns. Figure 5c shows the distribution of the conductance of the SWNT junctions with Au/Pd contacts. We achieved 99% and 100% yields using Au/Pd and Au/Ti electrodes, respectively. The average conductance of SWNT junctions with Au/Pd electrodes is ~40.00 μS, which is about an order of magnitude higher than that with Au/Ti electrodes (~4.086 μS). This higher conductance from the junctions with Au/Pd electrodes is attributed to reduced Schottky barriers as reported before[31].

Figure 5d shows the plot of conductance C versus effective thickness t of adsorbed SWNTs in SWNT junctions with Au/Pd electrodes. In this case, we could observe typical percolation behaviour in the SWNT networks. Using a log–log plot, we found a scaling behaviour of $C \approx t^{1.49}$, unlike in bulk materials, where the conductance C of a film is linearly proportional to its thickness t. Similar percolation behaviours have been reported using bulk-scale SWNT films[32]. We found slightly different behaviour from the junctions with Au/Ti electrodes (see Supplementary Information, Fig. S4). Their overall scaling behaviour looks similar to that of the Au/Pd electrode junctions. However, in the case of Au/Ti electrode junctions with a relatively small conductance of ~3 μS, the conductance and the effective thickness showed little correlation, implying that their conductance was mainly limited by the contact resistance.

In summary, we have developed a molecular linker-free directed assembly method, which allowed us to mass-produce high-performance NT- and NW-based devices using only conventional microfabrication facilities. As a proof of concept, we demonstrated wafer-scale assembly and alignment of SWNTs and V_2O_5 NWs on extremely versatile electronic substrates including Au, SiO_2, glass, Si and Al. Furthermore, we also performed wafer-scale fabrication of SWNT junctions and top-gate transistors with high yield and uniformity. After selective breakdown of metallic SWNTs, we were able to produce high-performance transistors with on–off ratios as large as $\sim 10^6$. As our method is readily accessible to the conventional electronics industry, it should open up immediate applications such as NT- and NW-based sensors, field-effect transistors and interconnectors.

METHODS

SUBSTRATE PREPARATION

SiO_2 and Si substrates were purchased from WaferMarket.com. Polycrystalline Au films were prepared by thermally depositing 10-nm-thick Ti layer followed by a 20-nm Au deposition on Si substrates under a high-vacuum condition (base pressure ~5×10^{-6} torr). Al films were prepared by thermally depositing a 20-nm-thick Al layer on Si substrates. Cover glass (Model: 12-548A) was purchased from Fisher Scientific.

SURFACE PASSIVATION

The CP-Research AFM (Digital Instruments) equipped with a temperature controller, a humidity controller, a closed-loop scanner and the DPN software (NanoInk) was used for AFM imaging and DPN experiments. 1-Octadecanethiol (ODT) and octadecyltrichlorosilane (OTS) SAM molecules and solvents were purchased from Sigma-Aldrich. The DPN and microcontact printing were used to deposit directly ODT molecules onto Au surfaces as reported previously[26–28]. To pattern OTS SAM on Si, glass, SiO_2 and Al surfaces, the photoresist (AZ1512) was first patterned on the substrates using a short baking time (<10 min at 95 °C) (Fig. 1b). The patterned substrate was then thoroughly rinsed with anhydrous hexane to remove adsorbed water on the substrate, and was immediately placed in the OTS solution (1:500 (v/v) in anhydrous hexane) for 100 s. Finally, the substrate was thoroughly rinsed with clean anhydrous hexane, and the photoresist was removed with acetone.

CARBON NT AND V_2O_5 NW ASSEMBLY

Purified SWNTs and fluorinated SWNTs (Carbon Nanotechnologies) were dispersed in 1,2-dichlorobenzene with ultrasonic vibration for 20 min to prepare a SWNT suspension. Two typical concentrations for SWNT suspensions were 0.2 mg ml^{-1} and 0.02 mg ml^{-1} or less. For SWNT assembly, the patterned surface was placed in the suspension, usually for 10 s, and rinsed thoroughly with 1,2-dichlorobenzene. V_2O_5 NWs were prepared as in the literature[12]. The assembly of V_2O_5 NWs was carried out by dipping the patterned substrate in the V_2O_5 NW solution, usually for 30 s. We used an Ag/AgCl (3.4 M KCl) reference electrode.

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Author contributions

M.L., J.I., and J.K. performed SWNT experiments and analyses: B.Y.L. performed NT-based biosensor experiments; S.M., M.L. and J.I. performed V_2O_5 NW experiments; Y.-K.K. and L.H. contributed to data analyses and interpretation of the results; and S.H. conceived and designed the experiments.

Competing financial interests

The authors declare that they have no competing financial interests.