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Voltage-switchable photocurrents in single-walled carbon nanotube–silicon junctions for analog and digital optoelectronics

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Recent progress in silicon photonics[1–8] has dramatically advanced the possible realization of heterogeneous logic circuits[9,10]. A variety of Boolean optoelectronic circuits have been proposed[11–15]. In this context, experimental investigation of logic operations with both optical and electrical inputs in chip-integrable devices is highly desirable. Here, we present a new kind of photodiode-based logic device using scalable heterojunctions of carbon nanotubes and silicon, the output currents of which can be manipulated completely by both optical and electrical inputs. This provides a novel platform for heterogeneous optoelectronic logic elements with voltage-switchable photocurrent responsivity of >1 A W^{-1}, photovoltage responsivity of >1 × 10^5 V W^{-1}, electrical on/off ratios of >1 × 10^5 and optical on/off ratios of >1 × 10^4. To demonstrate their scalability, we fabricated a large array of photoactive elements on a centimetre-scale wafer. We also present bidirectional phototransistors and novel clock-triggerable logic elements such as a mixed optoelectronic AND gate, a 2-bit optoelectronic ADDER/OR gate and a 4-bit optoelectronic digital-to-analog converter.

In recent times there has been remarkable progress in the development of silicon-based photonic circuit components such as on-chip sources, manipulators, detectors, storage, filtering and multiplexing technologies that are compatible with a microelectronics platform[1–8]. The successful integration of low-loss photonics-based data transfer technology with the performance of ultrafast logic and memory elements of conventional integrated circuits could provide new generations of microprocessors with significantly improved performances[9,16]. An important component of this heterogeneous integration would be the possible development of monolithic logic elements that can operate with both electrical and optical inputs. Historically, logic operations in electronic circuits are achieved using field-effect transistors[17,18], whereas the same in optical circuits can be achieved by methods such as second harmonic generation in nonlinear optical materials[19] and optomechanical resonance techniques[20]. To accomplish heterogeneous logic operations, a variety of hybrid logic elements using combinations of phototransistors, light-emitting diodes, waveguides and electro-optic switches have been suggested, taking advantage of the high-speed cascading Boolean algorithm of these optoelectronic circuits[11–15].

We show that heterojunctions of single-walled carbon nanotubes (SWNTs) and silicon can demonstrate a radically unconventional, sharply nonlinear, reverse-bias-dependent photocurrent, and this novel phenomenon provides a new way in which to obtain multifunctional analog and mixed digital optoelectronic operations with high switching ratios. Large switching of photocurrents can be obtained with small changes in voltage, enabling optoelectronic gates/devices with logic outputs depending on the logic state of both optical and electronic inputs. We demonstrate a number of novel optoelectronic switches/devices and the lithographic assembly of a large array of devices over a centimetre-scale wafer.

Figure 1a,b presents a schematic and a digital photograph of typical SWNT–Si test structures. Belts of SWNTs (height, ∼50 nm), with lateral sizes ranging from millimetres (Fig. 1b) to submicrometre (Fig. 1c), were assembled in a variety of configurations on lightly p-doped silicon surfaces using a template-assisted fluidic assembly method[21–23]. Similar heterojunctions have recently generated some interest in relation to solar cells[24,25] and photodetectors[26].

Under an applied voltage V, the current I in a conventional junction is expected to follow a diode rectification equation, $I(V) = I_s(e^{qV/\eta k_B T} - 1)$, where q, η, k_B and I_s are the electronic charge, ideality factor, Boltzmann constant and reverse saturation current, respectively[27]. When illuminated, the current follows the photodiode equation, $I(\mathrm{V}) = I_s(e^{qV/\eta k_B T} - 1) - I_{ph}$, where I_{ph} is the photocurrent, which usually depends on factors such as the incident photon flux and quantum efficiency, but has little or no dependence on the reverse bias. Figure 1d presents the dark and illuminated I–V curves for our SWNT–Si junctions, as well as the photocurrent response in a metal–silicon junction of similar dimensions. Although the dark I–V in the SWNT-Si junctions follows conventional rectification behaviour, the photocurrent clearly deviates from conventional behaviour, with a near-zero short-circuit current (independent of the incident power, see Supplementary Section 5) that sharply rises (by several orders of magnitude) within a few volts of reverse bias V_r. As seen in the same figure, this is strikingly different from the illuminated I–V of a conventional metal–Si Schottky junction of comparable dimensions, illuminated with the same light source. A proposed semi-quantitative model (see Supplementary Section 4) of the band structure of these heterojunctions reveals that the sharply nonlinear photocurrent behaviour is possibly related to the reverse-bias-tunable total number of available states in the SWNT belts, $n(\varepsilon = eV_r)$, for the photoexcited carriers to inject into from the silicon. Here, ε is the electronic energy measured from the effective Fermi level of the SWNT belt at thermal equilibrium. The inset of Fig. 1d compares I_{ph} and $n(\varepsilon)$ as a function of V_r and ε, respectively, demonstrating the close correlation between the two. As is evident from this model, at zero bias (short-circuit condition) $n(\varepsilon = 0) \approx 0$, so the short-circuit current is extremely low, independent of the incident power.

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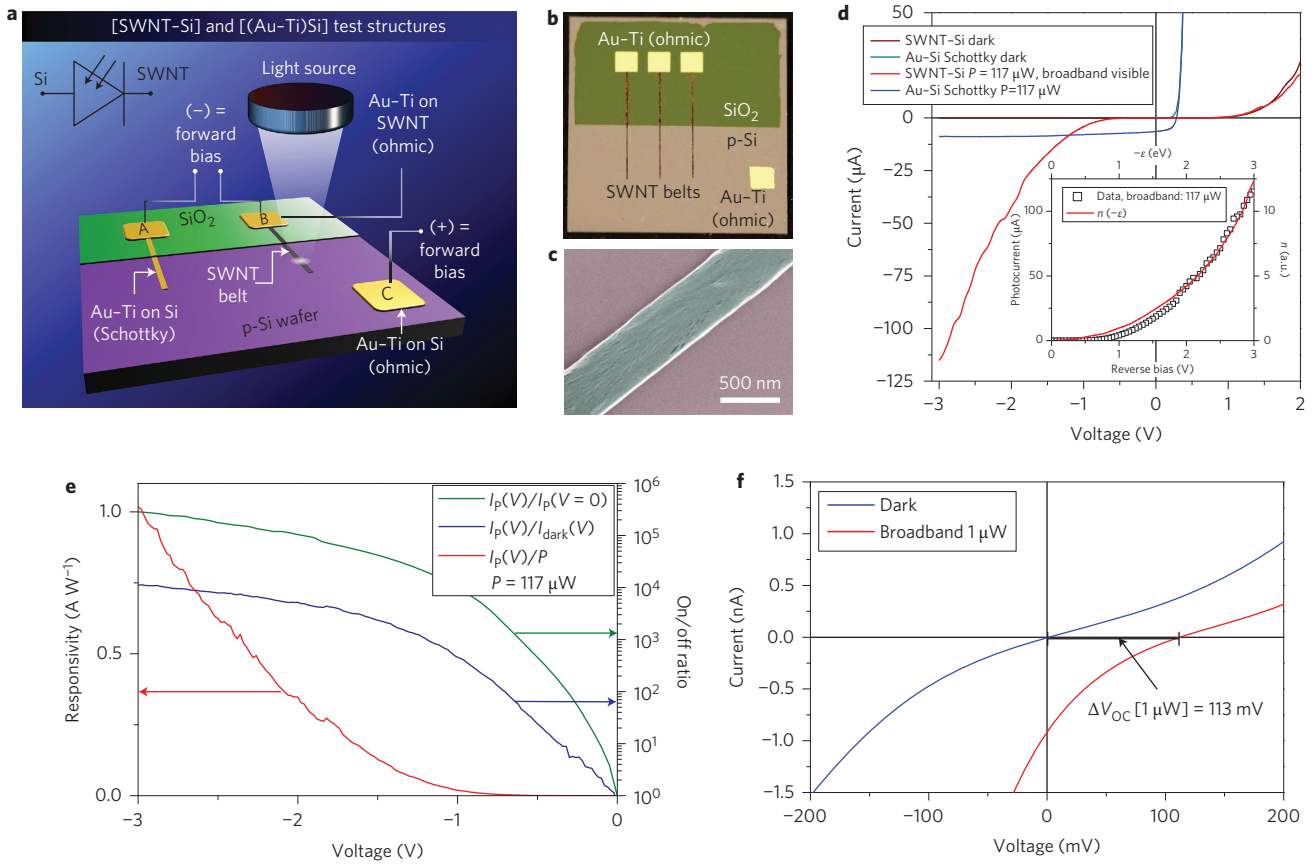

Figure 1 | Device structure and reverse-bias photoresponse. a,**b**, Schematic (**a**) and digital photograph (**b**) of a SWNT–Si heterojunction test structure (2 cm × 2 cm) with electrical contacts. The active region of each SWNT–Si junction has dimensions of 3 mm × 100 μm. **c**, Pseudo-coloured SEM image of a submicrometre-width fluidically assembled SWNT belt. **d**, Dark and illuminated *I*–*V* (117 μW broadband visible illumination; see Supplementary Section 5 for spectrum) curves of a typical SWNT–Si heterojunction. The dark and illuminated *I*–*V* curves of an Au–Ti–Si junction of similar dimensions and illumination condition is also shown for comparison of their shapes. Inset: comparison of the photocurrent data with a model describing the number of accessible states for photoexcited carriers *n* (see main text and Supplementary Section 4). **e**, Broadband responsivity and on/off ratios of the SWNT–Si junction as a function of the reverse bias. **f**, Change in open-circuit voltage under 1 μW illumination.

Figure 1e shows the variation of photocurrent responsivity $R = I_{ph}/P$ (P is incident power), electrical on/off ratio $I_P(V)/I_P(V=0)$ and optical on/off ratio $I_P(V)/I_{dark}(V)$ of the SWNT–Si junction. The maximum responsivity R_{max} obtained in our devices at low reverse bias (−3 V) exceeds 1 A W^{-1}, making them highly attractive both as photodetectors and as on-chip switching devices. Moreover, the response is completely tunable in the range $0 < R < R_{max}$ using very low voltages (−3 V to 0 V), which is extremely useful for sensitivity-adjustable imaging in variable light conditions, therefore making them quite attractive for imaging technologies. Also, the low dark current and incident power-independent low short-circuit currents coupled with this high responsivity at $V = -3$ V result in high electrical on/off ratios exceeding 2.5×10^5 and optical on/off ratios exceeding 1×10^4. Such high current-switching ratios are difficult to obtain in mixed-chirality SWNT arrays using purely electric field effects (gate voltage)[28].

Figure 1f shows the dark and $P = 1$ μW *I*–*V* curves in the SWNT–Si device. Under 1 μW incidence, the open-circuit voltage shifts by $\Delta V_{oc} = 113$ mV, which corresponds to a significantly large voltage responsivity of $R_V > 1 \times 10^5$ V W^{-1} and is orders of magnitude higher than past reports[29,30], making it extremely appealing for the design of low-power/portable weak-signal detection, imaging and on-chip analytical photochemistry applications.

Figure 2 summarizes the potential application of this tunable photoresponse in imaging technologies. The structural scalability and functional reproducibility of the fluidic assembly method is demonstrated by fabricating a large array of junctions on a 12 × 12 mm^2 area SiO_2/Si chip, designed to mimic the front end of a focal plane array. Figure 2a–c presents digital photographs of one such sensor array at different magnification levels, highlighting the large-scale integration achievable using our technique. The dense, uniform coverage of the circular silicon window without any stray suspended SWNTs or bubbles (as seen in Fig. 2d) is typical for all areas across the chip, and no structurally defective 'sensor' could be found under random scanning electron microscope (SEM) inspection of hundreds of sensors over the entire chip. Such a high degree of structural reproducibility is critical for large-area integration of sensors. Figure 2e shows a typical scanning photocurrent map of four pixels in a specially prepared chip where the front electrodes were lithographically shorted to a common external contact pad. The photocurrent maps show a uniform photoresponse from all the pixels (see Supplementary Section 6 for more detailed photocurrent map studies).

We next discuss examples of this junction being used as monolithic hybrid optical/electronic logic elements, for various analog and digital applications. Figure 3a shows inter-digitated SWNT belts connected to source and drain electrodes, equivalent to two back-to-back photodiodes forming a bidirectional phototransistor, as seen from the dark and illuminated *I*–*V* curves in Fig. 3b. In darkness, the device remains switched off for applied voltages of either polarity, while under illumination, an on state can be obtained for both positive and negative voltages. In this configuration, the

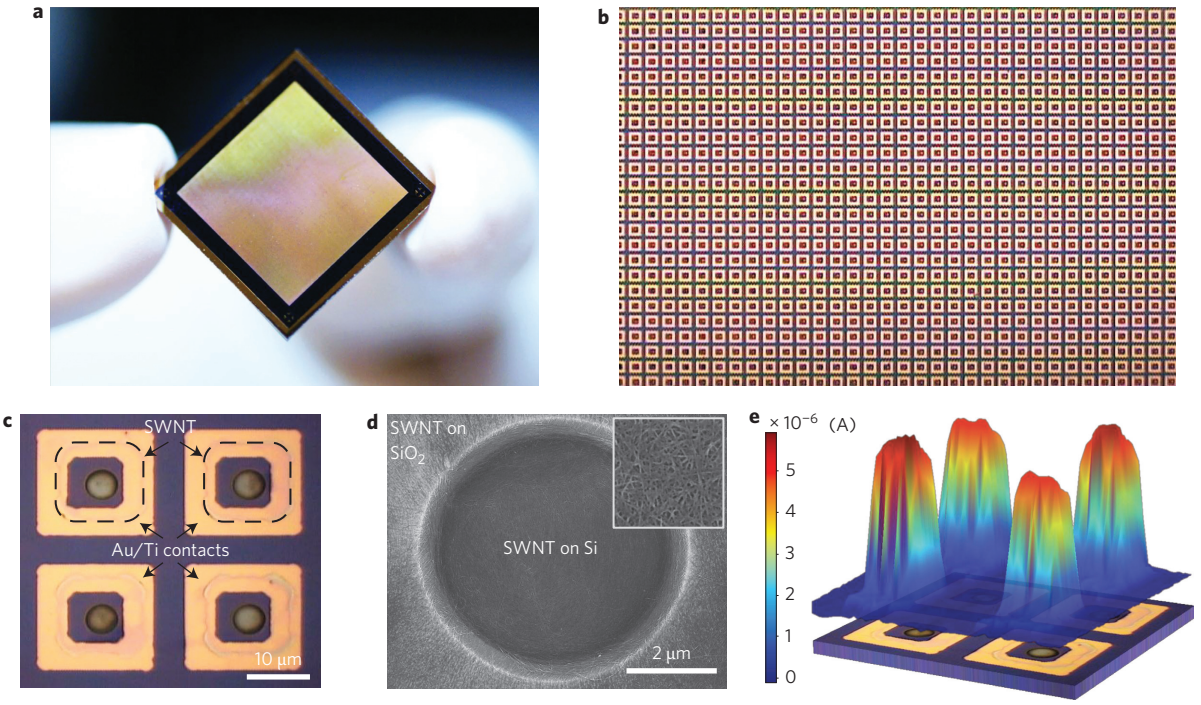

Figure 2 | Scalability and reproducibility. a, Digital photograph of a 0.25 megapixel array of SWNT–Si sensors (array area, 12 mm × 12 mm). **b**,**c**, The array of **a**, but with increasing levels of magnification. **d**, SEM image of the 'core' of the sensor, showing a circular window of silicon in a SiO_2/Si substrate overlaid with SWNTs. Inset: SEM image of the SWNT packing on silicon. **e**, Scanning photocurrent map ($\lambda = 532$ nm) of a 2 × 2 pixel area of the sensor array, where the pixels are electrically attached to an external lead and the back surface of silicon is used as the second contact.

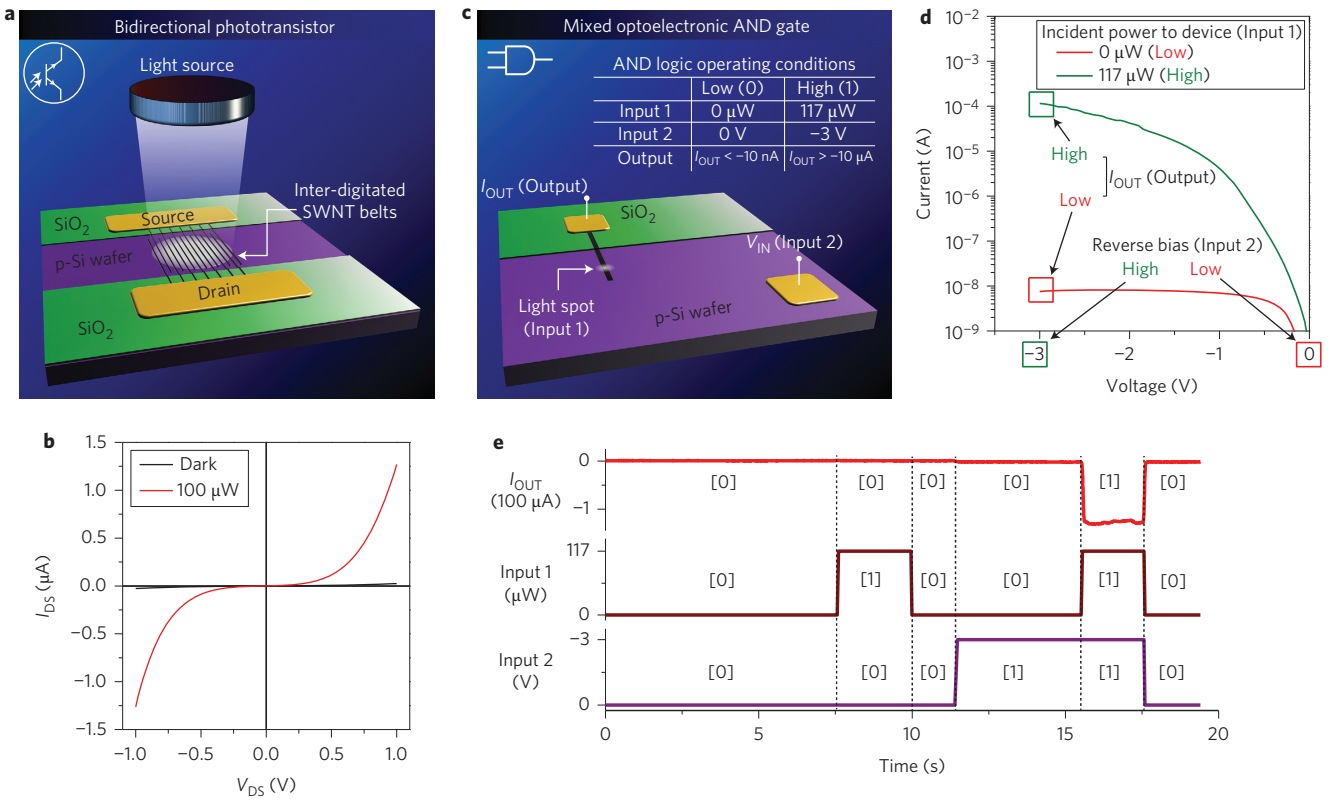

Figure 3 | Phototransistor and a hybrid logic gate. a, A bidirectional phototransistor using interdigitated SWNT fingers attached to source–drain leads. The active region of this device has an area of 3 mm × 200 μm. **b**, Typical *I*–*V* curve obtained in such a device under dark and illuminated conditions showing photo-induced on and off states. **c**, An AND gate with optical and electrical inputs and an electrical output. The active region of the junction has an area of 3 mm × 100 μm. Inset: a typical set of operating conditions determining the 'low' and 'high' logic states for both input and output conditions, as determined by the dark and photocurrents shown in **d**. **e**, Output of the AND gate for different input logic states as a function of time.

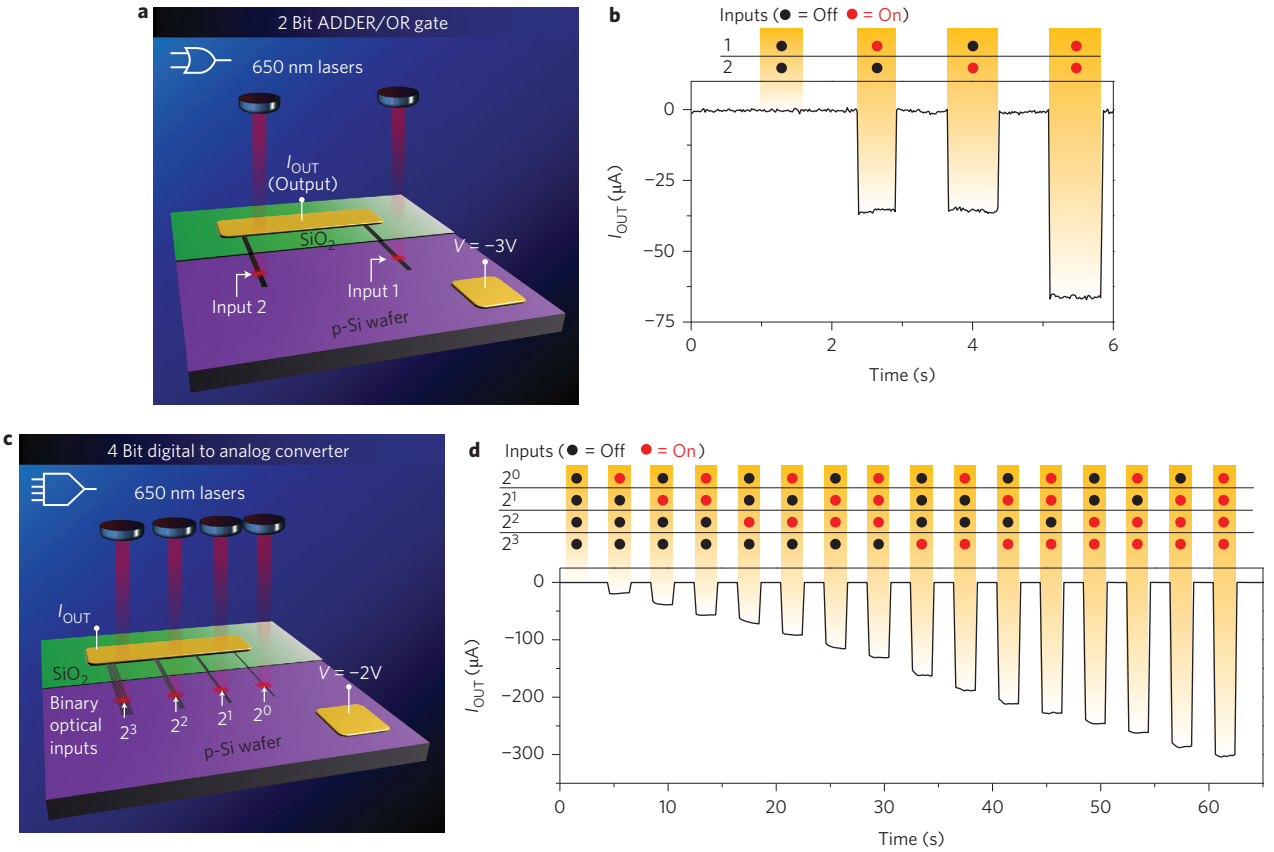

Figure 4 | Voltage-switchable 2-bit adder and a 4-bit digital-to-analog converter. a, Two identically fabricated SWNT–Si structures serving as independent optical inputs for an optoelectronic ADDER element. The active region of each input has an area of 3 mm × 100 μm. Two 650 nm lasers were used to independently address these two inputs. I_{OUT} is an analog electrical output signal that is proportional to the sum of the two digital inputs. Depending on the required operational condition, this element also doubles as an OR gate (see text). **b**, I_{OUT} versus time for different input configurations under an applied reverse bias. The red and black dots indicate the on and off states, respectively, of the two optical inputs. The output current shows a striking response reproducibility for independent illumination of the two structures, as does the current doubling when both inputs are illuminated simultaneously. This response reproducibility is crucial in designing scalable optoelectronic architectures such as the 4-bit optoelectronic digital-to-analog converter shown schematically in **c**. Each successive input has twice the number of (identical) SWNT belts (see text), corresponding to successive bit-significance, as shown. The active region of the 2^0 input is 2 mm × 50 μm. **d**, Analog current output corresponding to digital optical inputs ranging from binary 0000_2 (0_{10}) to 1111_2 (15_{10}). In both **a**,**b** and **c**,**d**, I_{OUT} can be completely turned off by turning off the reverse bias.

device is an optoelectronic equivalent of a symmetric field-effect transistor, but with the gate voltage replaced by photons. The applied voltage and incident light form two independent methods for controlling the channel current, both of which must be present to obtain an on state. This feature allows one to construct a mixed-input optoelectronic AND gate, as described in Fig. 3c. Here, the light spot incident on the SWNT–Si junction (input 1 measured in μW) and the applied bias (V_{IN}) are the two logic inputs, while the measured current output I_{OUT} is the logic output. The optical and electrical on and off states for a typical device can be obtained from the dark and illuminated I–V curves as shown in Fig. 3d; for convenience, these are tabulated in Fig. 3c. Figure 3e shows a typical time trace of the output state I_{OUT}, for different logic states of inputs 1 and 2, confirming its operation as a mixed optoelectronic AND gate.

Owing to the highly reproducible responsivity in different junctions fabricated in the same batch, our 'optical input–electronic output' devices are capable of operating with multiple optical inputs. Figure 4a shows a 2-bit, digital optical input, voltage-switchable analog output ADDER circuit, where the device adds two digital optical input signals and provides an output that is an analog equivalent of the digital sum. The calculation is performed only when a reverse bias is applied, which can be used as a clock trigger for the calculation. Under appropriate logic conditions, this also serves as an OR gate, and these operations can be seen in the output time trace for different input states in Fig. 4b. The high-fidelity adding operation can be extended to design more complex input bits by lithographically designing junctions with highly controlled surface areas. Figure 4c presents a voltage-switchable 4-bit optoelectronic digital-to-analog converter. To achieve this conversion, four separate SWNT–Si junctions with their junction areas proportional to 2^0, 2^1, 2^2 and 2^3 were designed (by fabricating one, two, four and eight parallel identical SWNT belts, respectively) to mimic the significant bits of a 4-bit optical input, each of which could be independently illuminated (or kept dark), resulting in binary inputs 0000–1111. The corresponding output, when triggered by a reverse bias, is the analog equivalent of these inputs, as seen in Fig. 4d, where—as a proof-of-principle—the analog reproduction of the binary inputs is quite remarkable.

Hence, SWNT–Si junctions form a versatile platform for optoelectronic applications ranging from photodetection, photometry and imaging. The voltage-switchable photocurrents with high switching ratios allow one to conceive mixed optoelectronic logic elements and voltage-triggered digital optoelectronic operations and digital-to-analog conversions. To our knowledge, this is the first demonstration of a monolithic device performing binary logic operations using a combination of optical and electrical inputs. The on-chip architectures are scalable and completely

compatible with conventional microelectronics technologies, including the possible inclusion of waveguides and other photonic components. Further developments in this field could pave the way for new approaches to integrating photonics into electronic circuits.

Methods

SWNTs of mixed chiralities were purchased commercially (Brewer Science CNTRENE) and assembled using a template-assisted fluidic assembly method as required on silicon and SiO_2 surfaces. Titanium/gold contacts were attached using standard lithographic techniques. The 0.25 megapixel detector array prototype was fabricated using a combination of lithographic and fluidic assembly steps. Photocurrent measurements were performed using a Keithley 2400 source meter, and the photocurrent maps were measured using an a.c. technique. A range of calibrated broadband and monochromatic light sources were used to test the devices. See Supplementary Information for detailed descriptions of these and other related topics.

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References

1. Almeida, V. R., Barrios, C. A., Panepucci, R. R. & Lipson, M. All-optical control of light on a silicon chip. *Nature* **431,** 1081–1084 (2004).
2. Vlasov, Y. A., Bo, X.-Z., Sturm, J. C. & Norris, D. J. On-chip natural assembly of silicon photonic bandgap crystals. *Nature* **414,** 289–293 (2001).
3. Vlasov, Y. A., O'Boyle, M., Hamann, H. F. & McNab, S. J. Active control of slow light on a chip with photonic crystal waveguides. *Nature* **438,** 65–69 (2005).
4. Liu, L. *et al.* An ultra-small, low-power, all-optical flip-flop memory on a silicon chip. *Nature Photon.* **4,** 182–187 (2010).
5. Rong, H. *et al.* A continuous-wave Raman silicon laser. *Nature* **433,** 725–728 (2005).
6. Hofmann, W. H., Moser, P. & Bimberg, D. Energy-Efficient VCSELs for interconnects. *IEEE Photon. J.* **4,** 652–656 (2012).
7. Michel, J., Liu, J. & Kimerling, L. C. High-performance Ge-on-Si photodetectors. *Nature Photon.* **4,** 527–534 (2010).
8. Bogaerts, W. *et al.* Silicon-on-insulator spectral filters fabricated with CMOS technology. *IEEE J. Sel. Top. Quantum Electron.* **16,** 33–44 (2010).
9. Liang, D., Roelkens, G., Baets, R. & Bowers, J. E. Hybrid integrated platforms for silicon photonics. *Materials* **3,** 1782–1802 (2010).
10. Lee, K.-W. *et al.* Three-dimensional hybrid integration technology of CMOS, MEMS, and photonics circuits for optoelectronic heterogeneous integrated systems. *IEEE Trans. Electron. Dev.* **58,** 748–757 (2011).
11. Krasilenko, V. G., Nikolsky, A. I., Lazarev, A. A. & Pavlov, S. N. Design and applications of a family of optoelectronic photocurrent logical elements on the basis of current mirror and comparators. *Proc. SPIE* **5948,** 59481G (2005).
12. Krasilenko, V. G., Ogorodnik, K. V., Nikolskyy, A. I. & Dubchak, V. N. Family of optoelectronic photocurrent reconfigurable universal (or multifunctional) logical elements (OPR ULE) on the basis of continuous logic operations (CLO) and current mirrors (CM). *Proc. SPIE* **8001,** 80012Q (2011).
13. Brackenbury, L. E. M. Optoelectronic differential multiplexer logic based on phototransistors/LEDs and its use in optical systems. *IEE Proc. Optoelectron.* **141,** 401–408 (1994).
14. Rao, E. S., Satyam, M. & Kishore, K. L. Electro-optical hybrid logic gates. *Semicond. Phys. Quantum Electron. Optoelectron.* **10,** 1740–1742 (2009).
15. Fetterman, M. R. Design for high-speed optoelectronic Boolean logic. *IEEE Photon. Technol. Lett.* **21,** 72–76 (2007).
16. Interconnect. CMOS-compatible optical interconnects and I/O, Section 5.3, page 58, in *International Technology Roadmap for Semiconductors*, 2011 edn; http://www.itrs.net/Links/2011ITRS/2011Chapters/2011Interconnect.pdf
17. Hofstein, S. & Heiman, F. The silicon insulated-gate field-effect transistor. *Proc. IEEE* **51,** 1190–1202 (1963).
18. Bertrand, G. *et al.* Towards the limits of conventional MOSFETs: case of sub 30 nm NMOS devices. *Solid-State Electron.* **48,** 505–509 (2004).
19. Stegeman, G., Hagan, D. & Torner, L. $\chi^{(2)}$ cascading phenomena and their applications to all-optical signal processing, mode-locking, pulse compression and solitons. *Opt. Quantum Electron.* **28,** 1691–1740 (1996).
20. Weis, S. *et al.* Optomechanically induced transparency. *Science* **330,** 1520–1523 (2010).
21. Jaber-Ansari, L. *et al.* Mechanism of very large scale assembly of SWNTs in template guided fluidic assembly process. *J. Am. Chem. Soc.* **131,** 804–808 (2009).
22. Xiong, X., Jaberansari, L., Hahm, M. G., Busnaina, A. & Jung, Y. J. Building highly organized single-walled-carbon-nanotube networks using template-guided fluidic assembly. *Small* **3,** 2006–2010 (2007).
23. Kim, Y. L. *et al.* Highly aligned scalable platinum-decorated single-wall carbon nanotube arrays for nanoscale electrical interconnects. *ACS Nano* **3,** 2818–2826 (2009).
24. Jia, Y. *et al.* Achieving high efficiency silicon–carbon nanotube heterojunction solar cells by acid doping. *Nano Lett.* **11,** 1901–1905 (2011).
25. Wadhwa, P., Seol, G., Petterson, M. K., Guo, J. & Rinzler, A. G. Electrolyte-induced inversion layer Schottky junction solar cells. *Nano Lett.* **11,** 2419–2423 (2011).
26. Behnam, A. *et al.* Experimental characterization of single-walled carbon nanotube film–Si Schottky contacts using metal–semiconductor–metal structures. *Appl. Phys. Lett.* **92,** 243116 (2008).
27. Sze, S. M. & Ng, K. K. *Physics of Semiconductor Devices* (Wiley-Interscience, 2006).
28. Seidel, R. W. *et al.* High-current nanotube transistors. *Nano Lett.* **4,** 831–834 (2004).
29. Wen, J. *et al.* High-sensitivity photovoltage based on the interfacial photoelectric effect in the $SrTiO_3-\delta$/Si heterojunction. *Sci. China Phys. Mech. Astron.* **53,** 2080–2083 (2010).
30. Wang, J., Hu, J., Becla, P., Agarwal, A. M. & Kimerling, L. C. Resonant-cavity-enhanced mid-infrared photodetector on a silicon platform. *Opt. Express* **18,** 12890–12896 (2010).

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Author contributions

Y.L.K., Y.J.J. and S.K. initiated the project and conceived the experiments. Y.L.K. fabricated and characterized the devices and analysed the data. H.Y.J. performed measurements and data analysis. B.L. fabricated devices and F.L. assisted with the optoelectronic measurement set-up. J.H. fabricated some of the devices in the final stages of the work. S.K. supervised the study with Y.-K.K. and Y.J.J. S.P. and Y.-K.K. simulated the results and proposed the device mechanism with S.K. All authors contributed to the analysis and commented on the work.

Additional information

Supplementary information is available in the online version of the paper. Reprints and permissions information is available online at www.nature.com/reprints. Correspondence and requests for materials should be addressed to Y-K.K., Y.J.J. and S.K.

Competing financial interests

At the time of submission, Northeastern University (Boston, USA) and Kyung Hee University (Seoul, Korea) were concurrently processing a patent application (PCT/US2013/60666).